REMARKS

This is in response to the Office Action dated August 6, 2003. Claims 2, 4, 6, 10, 20-28, 30 and 47-48 have been canceled. Claims 1, 3, 5, 7-9, 11-19, 29, 31-46 and 49-52 are now pending.

This amendment *should be entered* "after final" since it merely places subject matter from dependent claims into corresponding independent claims (i.e., no new issues are raised herein). In particular, subject matter of previous dependent claim 4 has been added to claim 1, claims 5 and 19 have been rewritten in independent form, subject matter of claim 38 has been added to claim 36, and subject matter of claim 48 has been added to claim 46. Thus, no new issues have been raised herein.

IDS Filings & Foreign Priority Claim

Initially, it is noted that applicant has not yet received initialed PTO-1449s corresponding to the IDS filings of July 18, 2003 and August 10, 2001. It is respectfully requested that the Examiner provide the undersigned with initialed PTO-1449 forms corresponding to these two IDS filings, so as to confirm their consideration.

Additionally, applicant notes that the Examiner has not yet acknowledged that "all" of the certified copies of the foreign priority documents have been received by the USPTO. Since applicant has in fact filed all such certified copies of the priority documents (on Aug. 10, 2001), it is respectfully requested that the Examiner acknowledge receipt of the same.

Example Non-Limiting Embodiments (for ease of understanding)

For purposes of example only, and without limitation, certain example embodiments of this invention relate to a semiconductor memory device. Referring to the embodiment of Figs. 1 and 73 for example, a semiconductor memory device includes a plurality of memory cells (e.g., EEPROMs) stacked on semiconductor substrate 100. As shown in Figs. 1 and 73, an example memory cell includes an island-shaped semiconductor layer(s) 110 which extends vertically relative to the semiconductor substrate 100, a charge storage layer(s) (e.g., floating gate 510), and a control gate(s) 520. It can be seen from Figs. 1 and 73 that the charge storage layer 510 (or 513) and the control gate 520 (or 523) laterally surround a vertically extending sidewall of island-like semiconductor layer 110 as viewed from above. Insulating layer 610 (or 613), including one or more insulators, is located between the control gate 520 (or 523) and the charge storage layer 510 (or 513). In Fig. 78, a pair of memory cells are located in the central portion of the stack, while first and second selection transistors using gate electrodes 500 are located at the top and bottom of the stack, respectively.

According to certain example non-limiting embodiments of this invention, the active region of at least one of the memory cells in the stack is electrically insulated form the semiconductor substrate 100 (e.g., pg. 47, lines 4-28; pg. 48, lines 4-18; pg. 92, lines 10-14; pg. 95, lines 11-27). In certain example embodiments, the active region of a memory cell may be electrically insulated from the semiconductor substrate by *both* (a) a diffusion layer formed in the semiconductor substrate or the island-like semiconductor

layer, and (b) a ***depletion layer*** formed at a junction between the diffusion layer and the semiconductor substrate or the island-like semiconductor layer. In the Fig. 97-98 embodiment, the island-like semiconductor layer 110 and the semiconductor substrate 100 become in an electrically floating state due to a *depletion layer* formed on the substrate or semiconductor layer of a PN junction formed between diffusion layer 710 and substrate 100 or semiconductor layer 110 by a difference between a potential given to diffusion layer 710 and a potential given to substrate 100 at times of reading and/or erasing (e.g., pg. 95, lines 11-27). Such structure is advantageous in that a back-bias effect in a semiconductor memory having charge storing layer(s) and control gate(s) can be reduced, and capacity between floating gates and control gates may be increased without significantly increasing the occupied area and variations in characteristics of memory cells may be suppressed (e.g., pg. 16, lines 19-24).

Claim 1

Claim 1 stands rejected under 35 U.S.C. Section 102(b) as being allegedly anticipated by Burns (US 5,990,509). This Section 102(b) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires that "the active region of said memory cell is electrically insulated from the semiconductor substrate by: (a) a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer and (b) a depletion layer formed at a junction between the second conductivity type impurity diffusion layer and the semiconductor substrate or the island-like semiconductor

layer." The cited art fails to disclose or suggest this aspect of claim 1 (i.e., previous claim 4).

Burns clearly fails to disclose or suggest the "depletion layer" recited in claim 1 for electrically insulating the active region of the memory cell from the semiconductor substrate. Burns discloses nothing akin to this aspect of claim 1, and is entirely unrelated thereto.

Other Claims

Burns also fails to disclose or suggest the claimed depletion layer recited in claims 5, 38 and 48 for electrically insulating the active region of the memory cell from the semiconductor substrate. Again, Burns is entirely unrelated to these claims in this respect.

Claim 19 requires that "a lower gate electrode of a selection transistor, the control gate of the memory cell, and an upper gate electrode of another selection transistor are arranged in an upward order in a direction vertical to the semiconductor substrate." For example, Fig. 73 of the instant application illustrates that a lower gate electrode 500 of a selection transistor, the control gate 520 of the memory cell, and an upper gate electrode 500 of another selection transistor are arranged in an upward order in a direction vertical to the semiconductor substrate 100.

Burns fails to disclose or suggest the aforesaid requirement of claim 19. Burns fails to discloses or suggest first and second selection transistors on opposite vertical

sides of at least one memory cell in a vertical direction as required by claim 19. Burns is entirely unrelated to the invention of claim 19 in this respect.

Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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